N-Channel and P-Channel Complementary MOSFET

Product Summary

NMOS

- V_{DS} 30V
- I_D 20A
- $R_{DS(ON)}$(at V_{GS}=10V) 30mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 50mΩ

PMOS

- V_{DS} -30V
- I_D -20A
- $R_{DS(ON)}$(at V_{GS}=-10V) 40mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) 60mΩ
- 100% EAS Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level ETQq0.000008882 0 596.04768 g0 G[ )]TJE

■ NMOS Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V	-	-	1	μA
		V_{DS}=30V, V_{GS}=0V, Tj=150	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ± 20V, V_{DS}=0V	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A	-	22	30	mΩ
		V_{GS}=4.5V, I_D=3A	-	37	50	
Diode Forward Voltage	V_{SD}	I_S=10A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	8	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	20	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz	-	235	-	pF
Output Capacitance	C_{oss}		-	43	-	
Reverse Transfer Capacitance	C_{rss}		-	35	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=15V,I_D=4A	-	6	-	nC
Gate-Source Charge	Q_{gs}		-	1.25	-	
Gate-Drain Charge	Q_{gd}		-	1.3	-	
Reverse Recovery Charge	Q_{rr}	I_F=4A, di/dt=100A/us				

NMOS Typical Electrical and Thermal Characteristics Diagrams

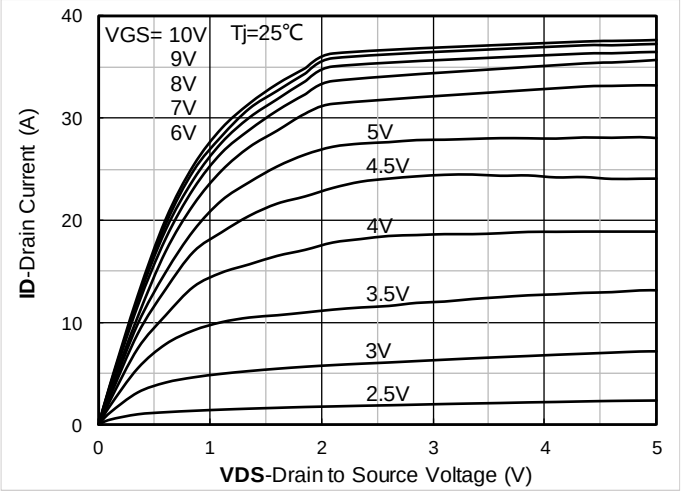


Figure 1. Output Characteristics

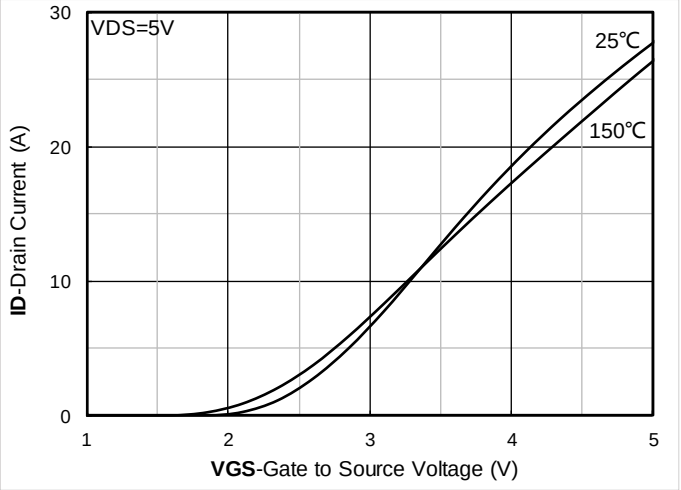


Figure 2. Transfer Characteristics

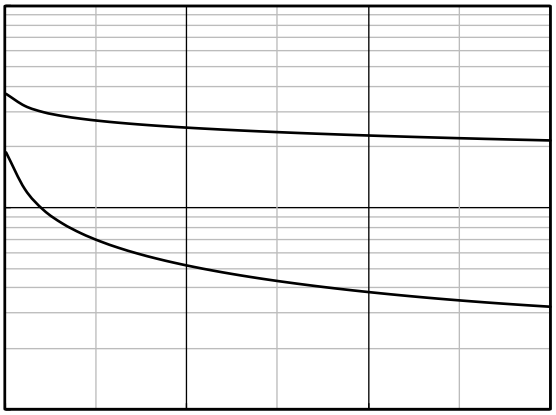


Figure 3. Capacitance Characteristics

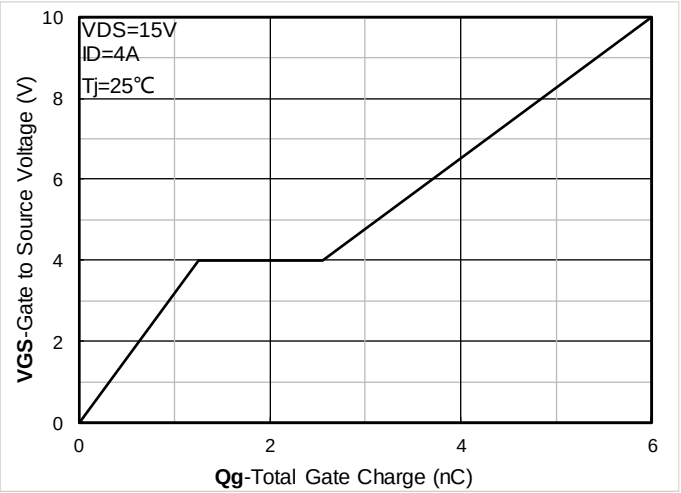


Figure 4. Gate Charge

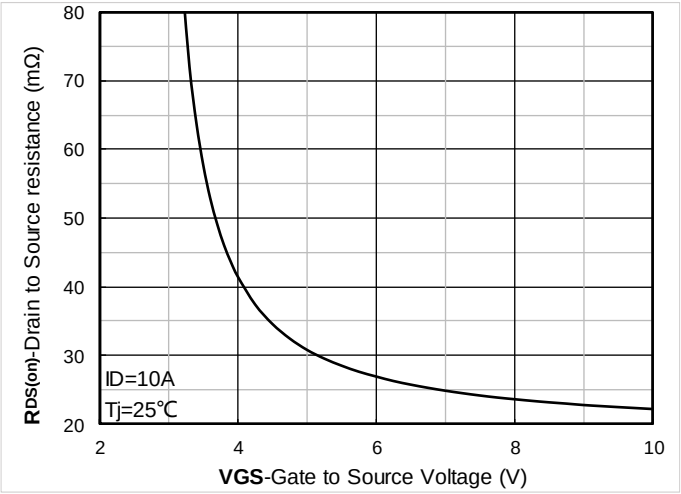


Figure 5. On-Resistance VS Gate to Source Voltage

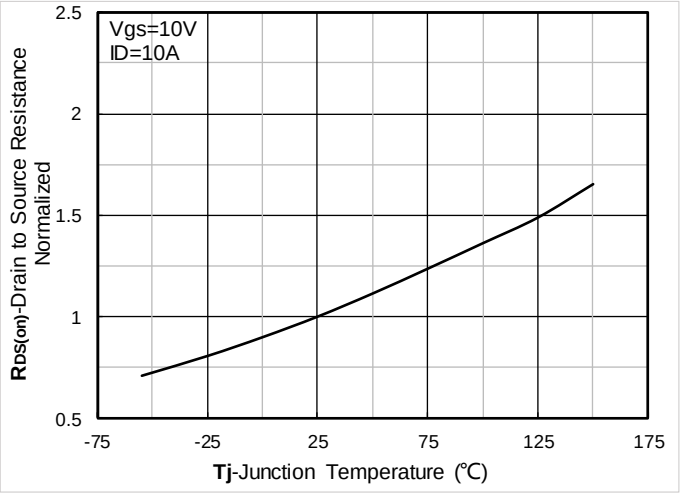


Figure 6. Normalized On- Resistance

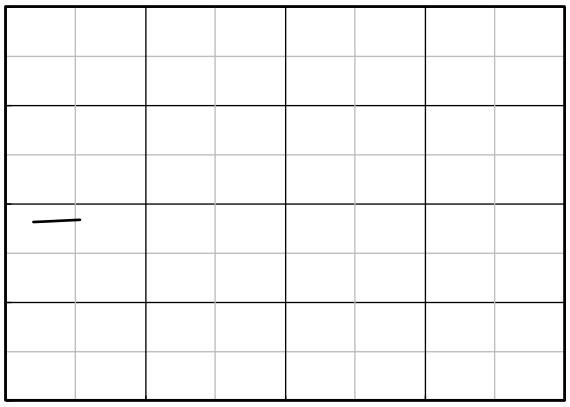


Figure 7. $R_{DS(on)}$ VS Drain Current

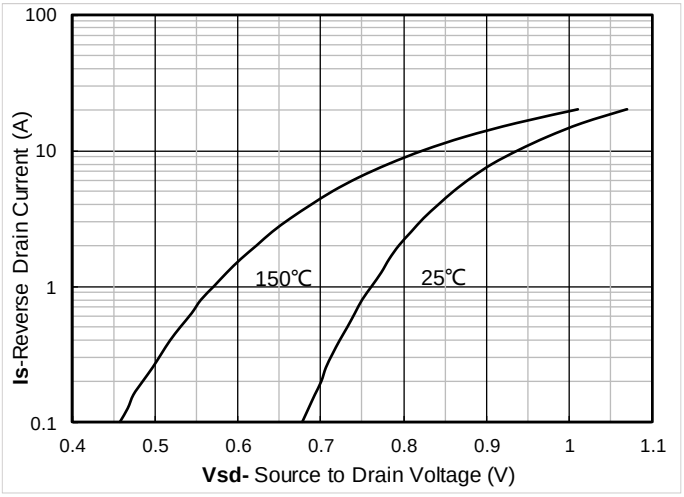


Figure 8. Forward characteristics of reverse diode

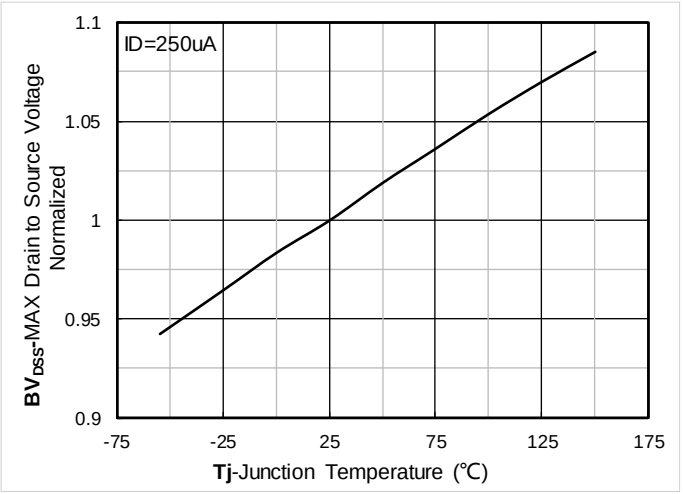


Figure 9. Normalized breakdown voltage

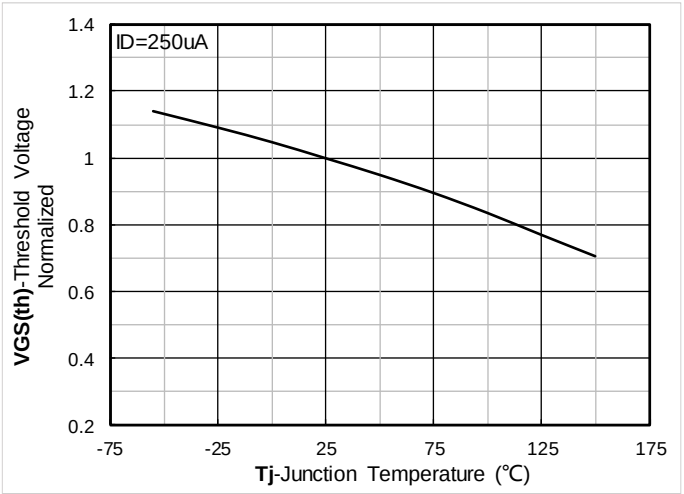


Figure 10. Normalized Threshold voltage

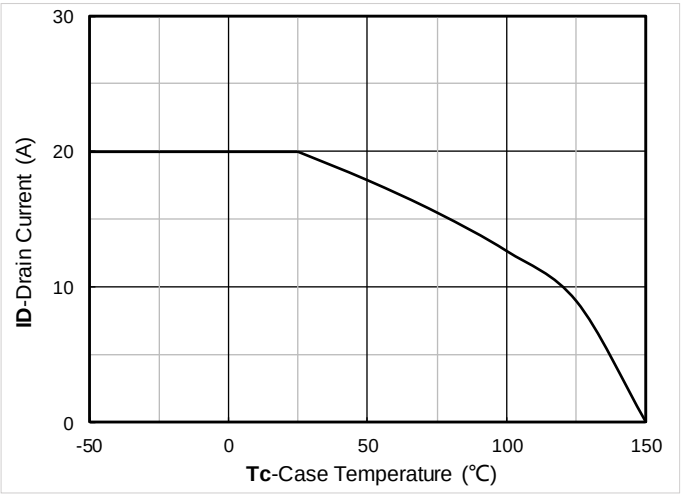


Figure 11. Current dissipation

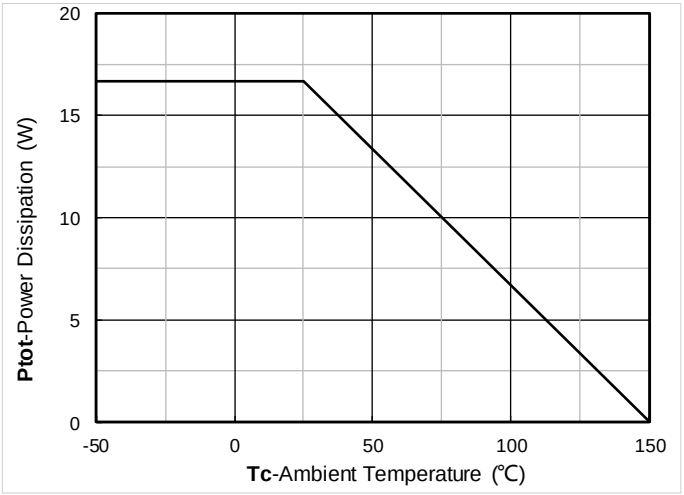


Figure 12. Power dissipation

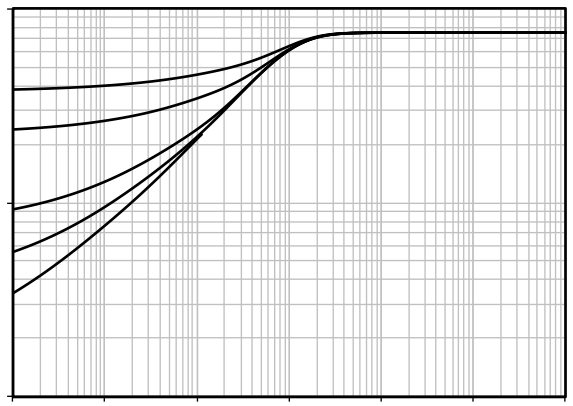


Figure 13. Maximum Transient Thermal Impedance

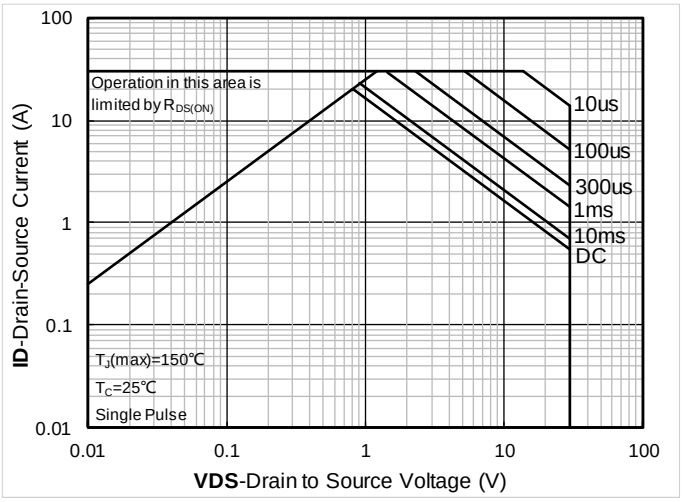


Figure 14. Safe Operation Area

PMOS Typical Electrical and Thermal Characteristics Diagrams

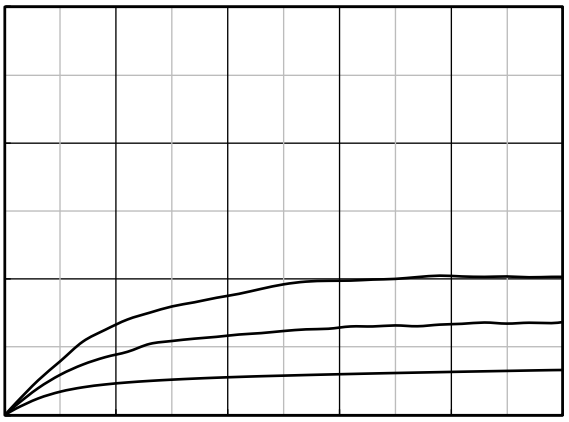


Figure 1. Output Characteristics

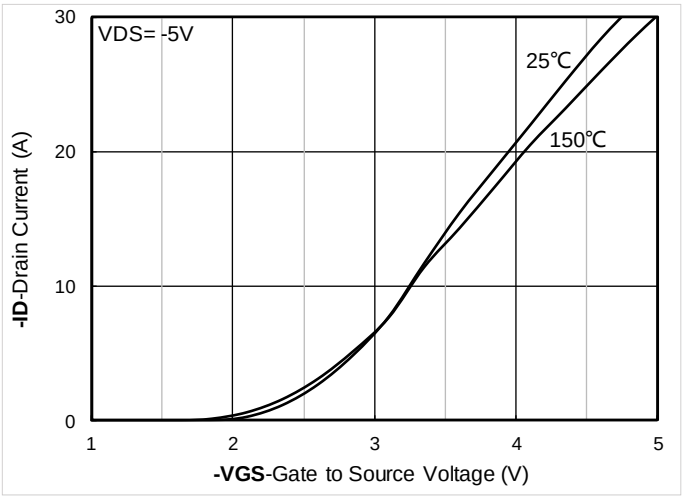
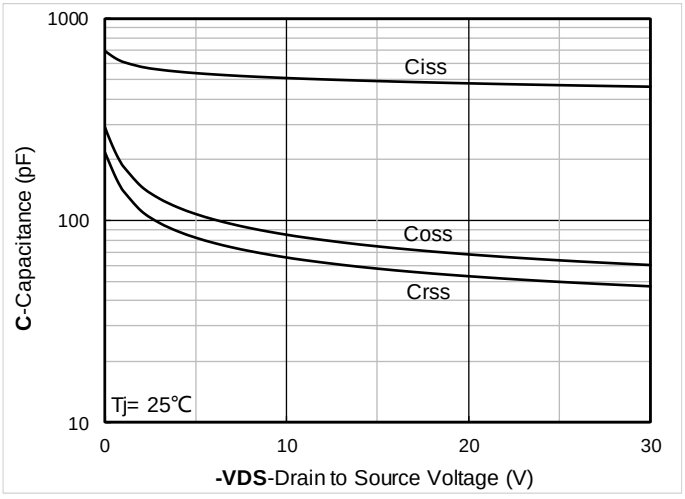


Figure 2. Transfer Characteristics



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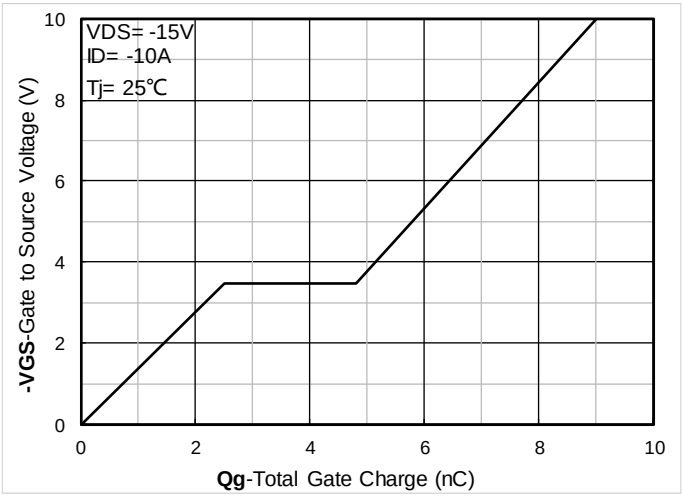


Figure 4. Gate Charge

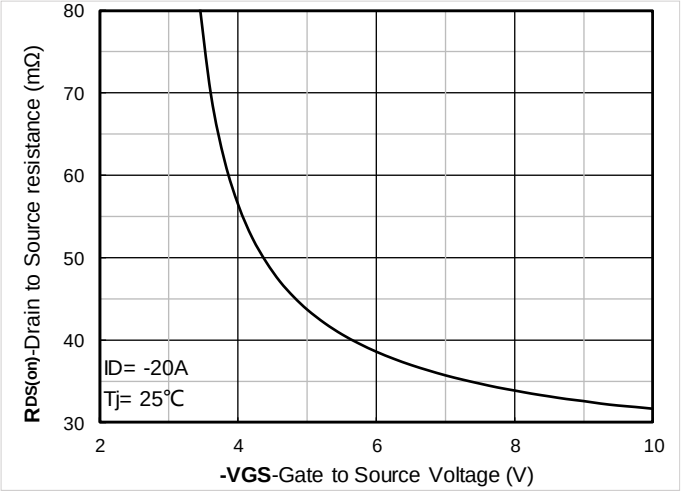


Figure 5. On-Resistance vs Gate to Source Voltage

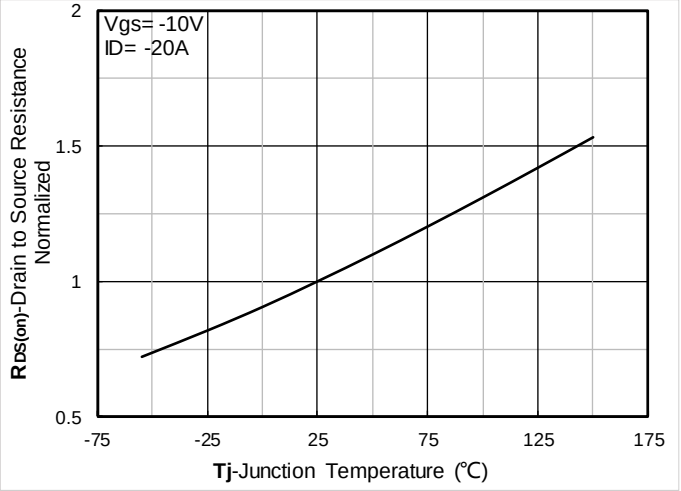


Figure 6. Normalized On-Resistance

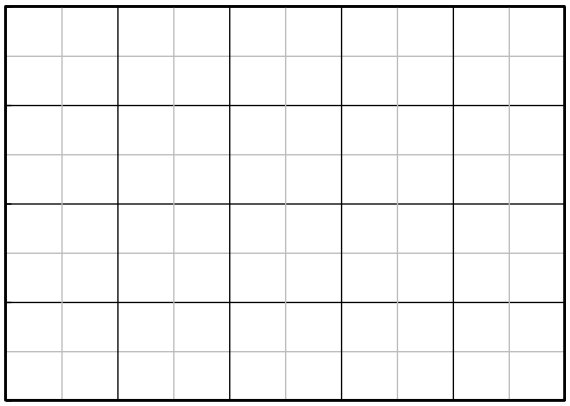
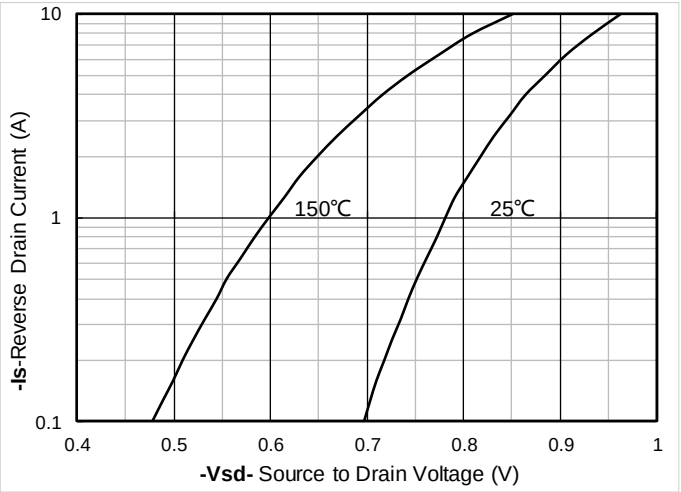


Figure 7. $R_{DS(on)}$ VS Drain Current



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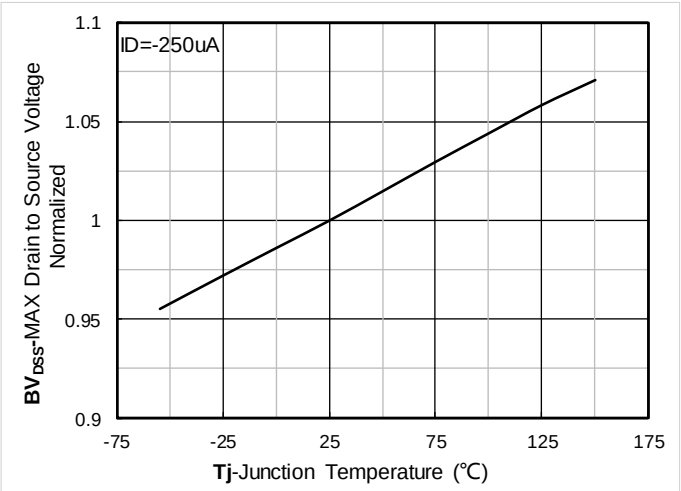


Figure 9. Normalized breakdown voltage

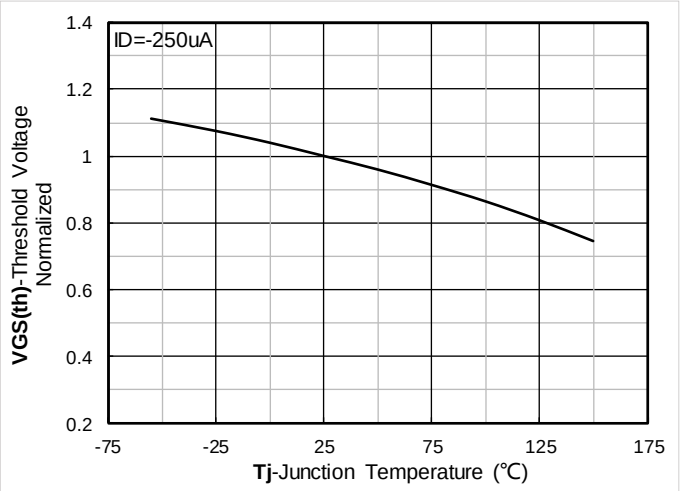


Figure 10. Normalized Threshold voltage

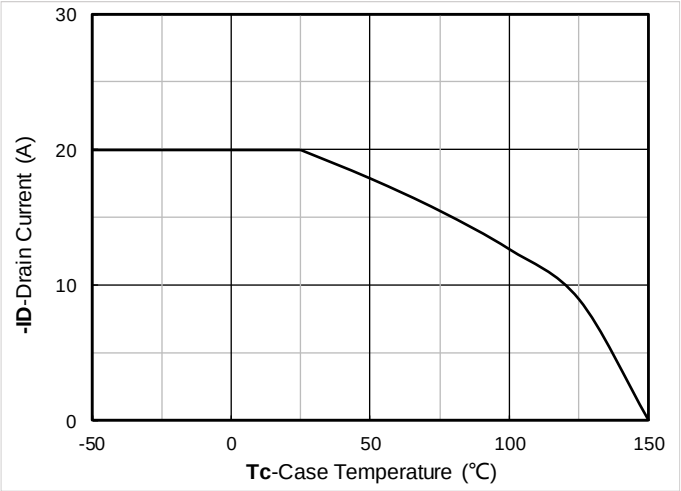


Figure 11. Current dissipation

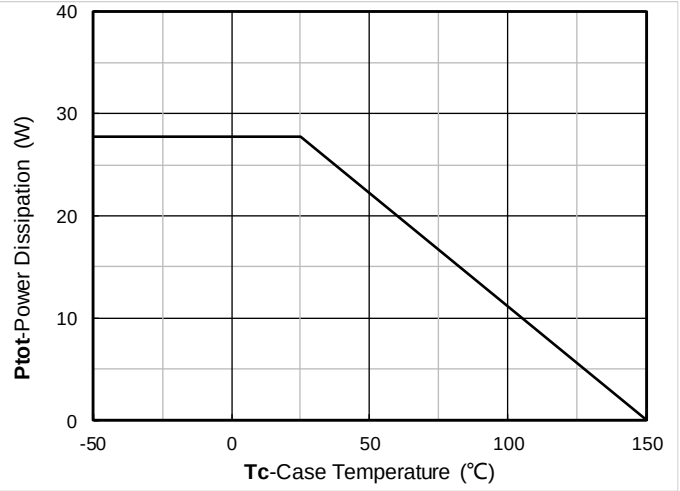
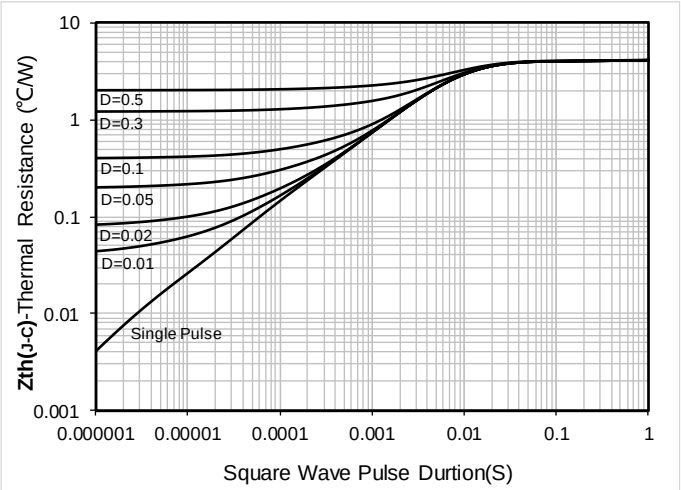


Figure 12. Power dissipation



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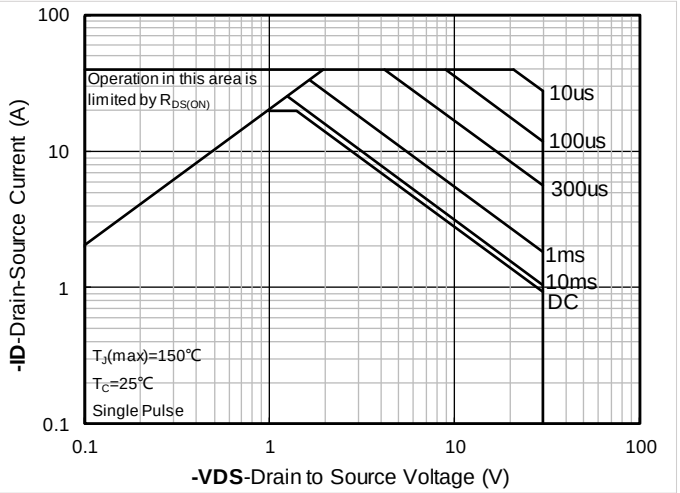
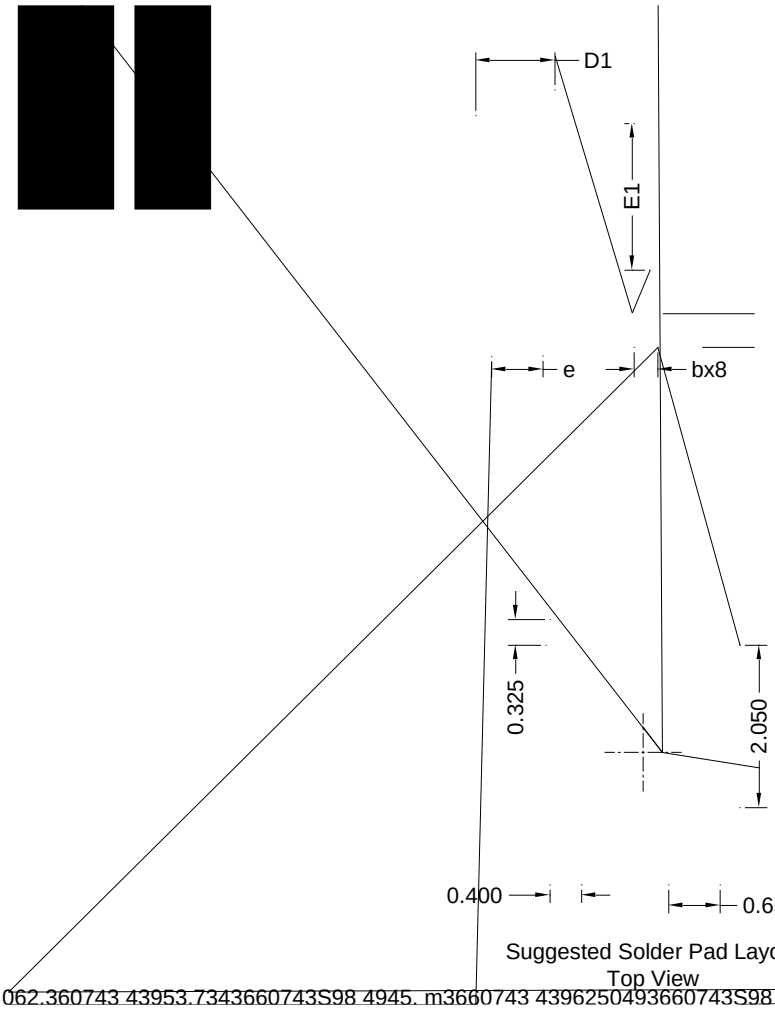


Figure 14. Safe Operation Area

■ DFN3333-8L-B-0.8MM Package information



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

062.360743 43953.7343660743S98 4945. m3660743 4396250493660743S98 49.3.43m3660743 43964.3660743S98 496942.3366074

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